JXT6966 / JXTS6966

6966-xxx

No. 87-0066969-002 Revision B

BIOS SETUP

TECHNICAL REFERENCE

Aptio® 4.x Test Setup Environment (TSE)

For use with JXT6966 or JXTS6966

Intel® Xeon® C5500-series

Quad-Core

PROCESSOR-BASED

SHB

WARRANTY

The following is an abbreviated version of Trenton Systems' warranty policy for PICMG® 1.3 products. For a complete warranty statement, contact Trenton or visit our website at www.TrentonSystems.com.

Trenton PICMG® 1.3 products are warranted against material and manufacturing defects for five years from date of delivery to the original purchaser. Buyer agrees that if this product proves defective Trenton Systems Inc. is only obligated to repair, replace or refund the purchase price of this product at Trenton Systems' discretion. The warranty is void if the product has been subjected to alteration, neglect, misuse or abuse; if any repairs have been attempted by anyone other than Trenton Systems Inc.; or if failure is caused by accident, acts of God, or other causes beyond the control of Trenton Systems Inc. Trenton Systems Inc. reserves the right to make changes or improvements in any product without incurring any obligation to similarly alter products previously purchased.

In no event shall Trenton Systems Inc. be liable for any defect in hardware or software or loss or inadequacy of data of any kind, or for any direct, indirect, incidental or consequential damages arising out of or in connection with the performance or use of the product or information provided. Trenton Systems Inc.'s liability shall in no event exceed the purchase price of the product purchased hereunder. The foregoing limitation of liability shall be equally applicable to any service provided by Trenton Systems Inc.

RETURN POLICY

Products returned for repair must be accompanied by a Return Material Authorization (RMA) number, obtained from Trenton Systems prior to return. Freight on all returned items must be prepaid by the customer, and the customer is responsible for any loss or damage caused by common carrier in transit. Items will be returned from Trenton Systems via Ground, unless prior arrangements are made by the customer for an alternative shipping method

To obtain an RMA number, call us at (800) 875-6031 or (770) 287-3100. We will need the following information:

Return company address and contact
Model name and model # from the label on the back of the product
Serial number from the label on the back of the product
Description of the failure

An RMA number will be issued. Mark the RMA number clearly on the outside of each box, include a failure report for each board and return the product(s) to our Utica, NY facility:

Trenton Technology Inc.
1001 Broad Street
Utica, NY 13501
Attn: Repair Department

Contact Trenton for our complete service and repair policy.

TRADEMARKS

IBM, PC/AT, VGA, EGA, OS/2 and PS/2 are trademarks or registered trademarks of International Business Machines Corp.
AMI, Aptio and AMIBIOS are trademarks of American Megatrends Inc.
Intel, Xeon, Intel Quick Path Interconnect, Intel Hyper-Threading Technology and Intel Virtualization Technology are trademarks or registered trademarks of Intel Corporation.
MS-DOS and Microsoft are registered trademarks of Microsoft Corp.
PICMG, SHB Express and the PICMG logo are trademarks or registered trademarks of the PCI Industrial Computer Manufacturers Group.
PCI Express is a trademark of the PCI-SIG
All other brand and product names may be trademarks or registered trademarks of their respective companies.

LIABILITY DISCLAIMER

This manual is as complete and factual as possible at the time of printing; however, the information in this manual may have been updated since that time. Trenton Systems Inc. reserves the right to change the functions, features or specifications of their products at any time, without notice.

E-mail: Support@TrentonSystems.com
Web: www.TrentonSystems.com

TRENTON SYSTEMS™
Engineered For Reliability

Trenton Systems, Inc.
2350 Centennial Drive • Gainesville, Georgia 30504
Sales: (800) 875-6031 • Phone: (770) 287-3100 • Fax: (770) 287-3150

This page intentionally left blank

Table of Contents

SHB HANDLING PRECAUTIONS

WARNING: This product has components which may be damaged by electrostatic discharge.

To protect your system host board (SHB) from electrostatic damage, be sure to observe the following precautions when handling or storing the board:

- Keep the SHB in its static-shielded bag until you are ready to perform your installation.
- Handle the SHB by its edges.
- Do not touch the I/O connector pins.
- Do not apply pressure or attach labels to the SHB.
- Use a grounded wrist strap at your workstation or ground yourself frequently by touching the metal chassis of the system before handling any components. The system must be plugged into an outlet that is connected to an earth ground.
- Use antistatic padding on all work surfaces.
- Avoid static-inducing carpeted areas.

RECOMMENDED BOARD HANDLING PRECAUTIONS

This SHB has components on both sides of the PCB. Some of these components are extremely small and subject to damage if the board is not handled properly. It is important for you to observe the following precautions when handling or storing the board to prevent components from being damaged or broken off:

- Handle the board only by its edges.
- Store the board in padded shipping material or in an anti-static board rack.
- Do not place an unprotected board on a flat surface.

This page intentionally left blank

Chapter 1 Starting Aptio® TSE

Introduction
The JXT6966 and JXTS6966 feature the Aptio® 4.x BIOS from American Megatrends, Inc. (AMI) with a ROM-resident setup utility called the Aptio® Text Setup Environment or TSE. The TSE allows you to select to the following categories of options:

- Main Menu
- Advanced Setup
- Boot Setup
- Security Setup
- Chipset Setup
- Exit

Each of these options allows you to review and/or change various setup features of your system. Details are provided in the following chapters of this manual. Additional copies of the Trenton JXT6966 / JXTS6966 BIOS and hardware technical reference manuals are available under the **Downloads** tab on the JXT6966 or JXTS6966 web pages.

Aptio Text Setup Environment (TSE) is a text-based basic input and output system. The purpose of Aptio TSE is to empower the user with complete system control at boot. This document explains the basic navigation of Aptio TSE.

NOTE: The contents of this document were provided as a courtesy from American Megatrends, Inc. or AMI and describe the standard look and feel of the Aptio TSE interface. Trenton Systems Inc. is the manufacturer of the SHB hardware and during production may have made subtle changes to some of the settings described in this document. Therefore, some of the options that are described in this document may not exist or may have been modified for use in the JXT6966 / JXTS6966 implementation of the Aptio TSE BIOS utility. Contact Trenton Technical support for any questions regarding the SHBs' implementation of Aptio TSE.

Starting Aptio TSE
To enter the Aptio TSE screens, follow the steps below:

Step	Description
1	Install the SHB in a PICMG 1.3 backplane with the proper system power connections made to the backplane and a mouse, keyboard and monitor connected to the SHB
2	Power on the system with the SHB
3	Press the <Delete> or <F2> key on your keyboard when you see the following text prompt: **Press DEL or F2 to enter Setup**
4	After you press the <Delete>/<F2> key, the Aptio TSE main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu, such as the Chipset and Power menus.

NOTE: In most cases, the <Delete> or <F2> keys are used to invoke the Aptio TSE screen. There are a few cases that other keys are used (<F1>, <F10>, …).

NOTE: The user can press the <TAB> key during boot to switch from the boot splash screen (logo) to see the keystroke messages.

Aptio® TSE Setup Menu

The Aptio TSE BIOS setup menu is the first screen that you can navigate. Each BIOS setup menu option is described in this user's guide.

Aptio Setup Utility – Copyright © 2009 American Megatrends Inc.						
Main	Advanced	Chipset	Boot	Security	Save & Exit	Event Logs
BIOS Information					**Choose the system default language**	
BIOS Vendor	American Megatrends					
Core Version	4.6.3.7					
Project Version	0ABWD 0.22x64					
Build Date	08/17/2011					
Customer Reference Number	006250					
Memory Information						
Total Memory	4096 MB (DDR3)					
System Language	**[English]**				→← : Select Screen	
					↑↓ : Select Item	
System Date	[Thu 11/02/2012]				Enter: Select	
System Time	[14:20:00]				+/- : Change Opt.	
					F1 : General Help	
Access Level	Administrator				F2 : Previous Values	
					F3 : Optimized Defaults	
					F4 : Save & Exit	
					ESC : Exit	
Version 2.00.1201, Copyright © 2009 American Megatrends, Inc.						

There may be slight differences in the screen shots illustrated in this manual due to Trenton JXT6966 BIOS modifications. Contact Trenton Technical support for any questions regarding the SHBs' implementation of Aptio TSE.

Navigation

The Aptio® TSE keyboard-based navigation can be accomplished using a combination of the keys.(<FUNCTION> keys, <ENTER>, <ESC>, <ARROW> keys, etc.).

Key	Description
ENTER	The *Enter* key allows the user to select an option to edit its value or access a sub menu.
→← Left/Right	The *Left and Right* <Arrow> keys allow you to select an Aptio TSE screen. For example: Main screen, Advanced screen, Chipset screen, and so on.
↑↓ Up/Down	The *Up and Down* <Arrow> keys allow you to select an Aptio TSE item or sub-screen.
+- Plus/Minus	The *Plus and Minus* <Arrow> keys allow you to change the field value of a particular setup item. For example: Date and Time.
Tab	The <Tab> key allows you to select Aptio TSE fields.
ESC	The <Esc> key allows you to discard any changes you have made and exit the Aptio TSE. Press the <Esc> key to exit the Aptio TSE without saving your changes. The following screen will appear: Press the <Enter> key to discard changes and exit. You can also use the <Arrow> key to select *Cancel* and then press the <Enter> key to abort this function and return to the previous screen.
Function keys	When other function keys become available, they are displayed in the help screen along with their intended function.

This page intentionally left blank

Chapter 2 Advanced Setup

Introduction
Select the *Advanced* menu item from the Aptio TSE screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as System Launch Settings, PCI Sub-System Configuration, ACPI Settings, CPU Configuration, SATA/IDE Configuration, USB Configuration, Info Report Configuration, SuperIO Configuration and Serial Port Redirection.

Aptio Setup Utility – Copyright © 2009 American Megatrends Inc.						
Main	**Advanced**	Chipset	Boot	Security	Save & Exit	Event Logs
Legacy OpRom Support					**Enable of Disable Boot Option for Legacy Devices**	
Launch PXE OpRom		**Disabled**/Enabled				
Launch Storage OpRom		Enabled/Disabled				
►PCI Subsystem Settings					→← : Select Screen	
►ACPI Settings					↑↓ : Select Item	
►CPU Configuration					Enter: Select	
►Runtime Error Logging					+/- : Change Opt.	
►SATA Configuration					F1 : General Help	
►USB Configuration					F2 : Previous Values	
►Info Report Configuration					F3 : Optimized Defaults	
►SuperIO Configuration					F4 : Save & Exit	
►Serial Port Console Redirection					ESC : Exit	
					F1 : General Help	
Version 2.00.1201, Copyright © 2009 American Megatrends, Inc.						

Note: The board needs to have the optional IOB33 installed for the SuperIO Configuration and Serial Port Redirection selections to appear on the Advanced BIOS selection screen.

Here is a short description of the Advanced BIOS selections:

Launch PXE OpROM Configuration
With this selection, you can enable or disable the system's Boot From LAN capability of the SHB which allows system ROM storage settings for legacy networks. Available settings are **Disabled**/Enabled with the Disable option being the default settings. Note: **Bold text** indicates the BIOS default setting.

Launch Storage OpROM Configuration
With this selection, you can **enable** or disable the system's ROM storage settings for legacy mass storage devices.

PCI Subsystem Settings
Various device settings are available for configuration with this BIOS parameter. Specific device availability depends on what the BIOS can see during the system boot process.

ACPI Settings
This is where you set up your system for use with the ACPI soft control states available on the SHB. Various system sleep states and recover modes are available for selection on this sub-menu..

CPU Configuration
The parameters for the specific Jasper Forest processors installed on your SHB are displayed on the top portion of this sub-menu. The lower portion of this screen contains processor features that you may elect to enable or disable on the unique requirements of your system. Here is a partial listing of some of these CPU parameters.

Option	Description
Intel® Hyper-Threading	This option allows the user to enable or disable Intel® Hyper-Threading support on the Intel® Xeon® C5000 series (i.e. Jasper Forest) processor. By default, this setting is enabled.
Intel® Virtualization	This option allows the user to enable or disable Intel® Virtualization support on the Intel® Xeon® C5000 series (i.e. Jasper Forest) processor. By default, this setting is enabled.
Execute Disable Bit	This option allows the user to enable or disable Intel® Execute Disable Bit feature of the Intel® Xeon® C5000 series (i.e. Jasper Forest) processor.
Active Processor Cores	With this setting you may us all of the available cores available in the Intel® Xeon® C5000 series (i.e. Jasper Forest) processor or on use a subset of the available CPU execution cores. The default setting for this option is "ALL" and the number of cores to select depends on the specific processor installed on the SHB.

Runtime Error Logging
Used to enable or disable the processor's error control bit.

SATA Configuration
This is where you can set the parameters for the SATA devices that have been sensed SHBs' during the boot process.

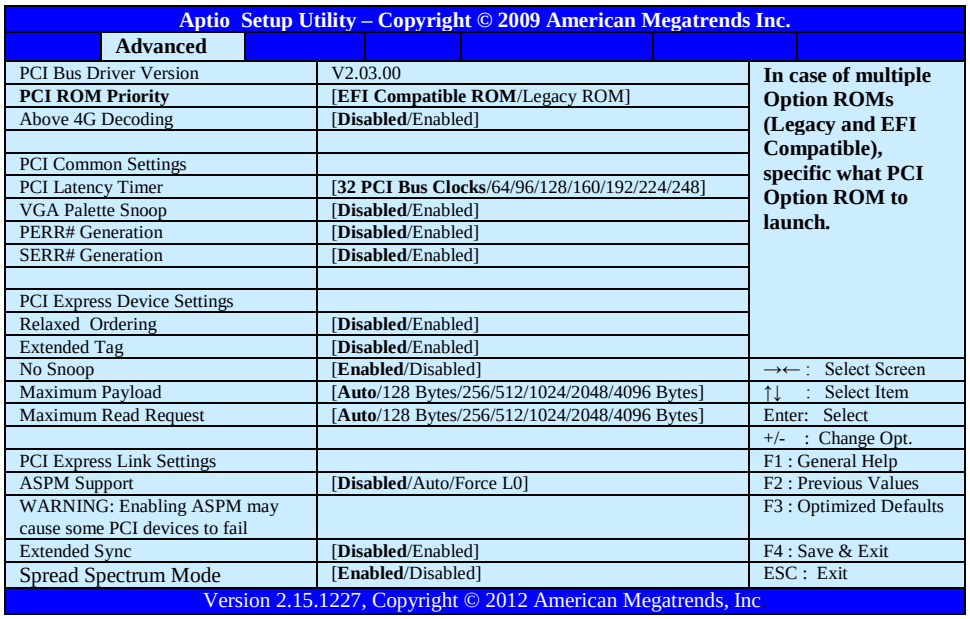
USB Configuration
This is where you can set the parameters for the USB devices that have been sensed SHBs' during the boot process.

Info Report Configuration
This is where you can set the parameters have the SHB enable selected system BIOS reports.

Super IO Configuration
The only Super IO component available in a system implementation using a JXT6966 or JXTS6966 is located on the optional IOB33 module. An IOB33 can plug into the SHBs' P20 I/O Expansion connector. If an IOB33 is plugged into the SHB then the Super IO Configuration submenu will be displayed

Serial Port Console Redirection
The SHB must have an optional IOB33 installed in order for the BIOS setting to apply. Serial port console redirection is available for use on the IOB33's COM0 and COM1 serial communication ports.

Selecting one of the set-up items in the Advanced BIOS selection screen such as the **PCI Subsystem Settings** results in the sub-menu screen illustrated below.



PCI Sub-System Settings

A number of PCI Express, PCI-X and PCI device settings are available for configuration with this BIOS parameter. Specific device availability depends on what the BIOS can see during the system boot process. The PCI Subsystem Setting is used to optimize the operations of off-board cards or devices that interact with the SHB and the SHB's BIOS. Listed below are all the available BIOS settings for board's PCI bus driver and the PCI Express link interfaces.

Option	Description
PCI ROM Priority	**EFI Compatible ROM**/Legacy ROM **(bold** = default setting)
Above 4G Decoding	**Disabled**/Enabled – The system design needs to support 64-bit PCI decoding for this setting to be meaningful. Enabling the setting allows the SHB to decode the 64-bit capable devices connected to the SHB the 4G-address space. Use caution when enabling this system BIOS parameter.
PCI Latency Timer	Timer value selections available: **32 PCI Bus Clocks**, 64 PCI Bus Clocks, 96 PCI Bus Clocks, 128 PCI Bus Clocks, 160 PCI Bus Clocks, 192 PCI Bus Clocks, 224 PCI Bus Clocks, 248 PCI Bus Clocks
VGA Pallet Snoop	**Disabled**/Enabled
PERR# Generation	**Disabled**/Enabled
SERR# Generation	**Disabled**/Enabled
PCI Express Device Settings	There are several sections associated with this BIOS parameter setting as shown below. Short operational descriptions for each setting can be found in the upper left corner of the BIOS set-up screen. PCI Express Device Register Settings Relaxed Ordering: ***Disabled****/Enabled* **(bold** = default setting) Extended Tag: **Disabled**/Enabled No Snoop: Disabled/**Enabled** Maximum Payload: **Auto**, 128 Bytes, 256 Bytes, 512 Bytes, 1024 Bytes, 2048Bytes, 4096 Bytes Maximum Read Request: **Auto**, 128 Bytes, 256 Bytes, 512 Bytes, 1024 Bytes, 2048Bytes, 4096 Bytes
PCI Express Link Settings	ASPM Support: **Disabled**/Auto/Force L0 WARNING: Enabling ASPM may cause some PCI devices to fail Extended Sync: **Disabled**/Enabled Spread Spectrum Mode: *Disabled/****Enabled***

ACPI Settings

This is where you set up your system for use with the ACPI soft control states available on the SHB. The standard BIOS default is the S3 (Suspend to RAM) sleep state. The SHB hardware and BIOS supports both the S1 and S3 sleep states and are available for selection at the operating system level.

Option	Description
Enable ACPI Auto Configuration	**Disabled**/Enabled **(bold** = default setting)
Enable Hibernation	Disabled/**Enabled**
ACPI Sleep State	**S3 (Suspend to RAM)**/Suspend Disabled/S1 (CPU Stop Clock)
S3 Video Repost	**Enabled**/Disabled
Power Supply Shutoff	**AUTO**/Manual

CPU Configuration

The first six settings on the sub-menu display the specifics of the processors installed in the SHB sockets. The remaining selections provide the mechanism to enable or disable select processor features.

Option	Description
Processor Type	Intel® Xeon® CPU
EMT64	Supported
Processor Speed	2128 MHz
Processor Stepping	106e4
Processor Cores	4
Intel HT Technology	Supported
Hyper-Threading	**Enabled**/Disabled (**bold** = default setting)
Active Processor Cores	**All**/1/2
Limit CPUID Maximum	**Disabled**/Enabled
Execute Disable Bit	**Enabled**/Disabled
Hardware Prefetcher	**Enabled**/Disabled
Adjacent Cache Line Prefetch	**Enabled**/Disabled
Intel Virtualization Technology	**Disabled**/Enabled
Power Technology	Energy Efficient/Disable/Custom
EIST	**Enabled**/Disabled
Turbo Mode	**Enabled**/Disabled
Performance/Watt	**Traditional**/Power Optimized
P-State Coordination	**HW_ALL**/SW_ALL/SW_ANY
CPU C3 Report	**Disabled**/ACPI C-2/ACPI C-3
CPU C6 Report	**Enabled**/Disabled
CPU C7 Report	**Enabled**/Disabled
Interrupt Filtering	**Enabled**/Disabled
Package C State Limit	**No Limit**/C0/C1/C3/C6/C7
Local x2APIC	**Disabled**/Enabled
TDC Limit	**0**
TDP Limit	**0**
1-Core Ratio Limit	**0**
2-Core Ratio Limit	**0**
3-Core Ratio Limit	**0**
4-Core Ratio Limit	**0**

Runtime Error Logging Configuration
Also called "Windows Hardware Error Architecture", this menu selection is used to enable or disable the runtime error logging support feature and its associated operational parameters.

Option	Description
Runtime Error Logging	**Disabled**/Enabled **(bold** = default setting) - If enabled the following sub-menu option choices are available: PCI Error Logging Support: ***Disabled****/Enabled* PCI AER Logging Support: ***Disabled****/Enabled* Corr. Error Threshold: ***10*** Short operational descriptions for each sub-menu setting can be found in the upper left corner of the BIOS set-up screen.

SATA Configuration
This is where you can set the parameters for the SATA devices that have been sensed by the SHB during the boot process. SATA devices connected to ports P27, P28, P31, P32, P35 or P36 have a maximum data transfer rate of 300MB/s. What follows is a list of SATA port configuration parameters.

Option	Description
SATA Port0 through SATA Port5	SATA Port0 through 5 will display the specific for a SATA drive connected to P27 (SATA0), P28 (SATA1), P31 (SATA2), P32 (SATA3), P35 (SATA4) or P36 (SATA5). If a drive is not connected to a port that the message *Not Present* will be displayed.
SATA Mode	Disabled/**IDE Mode**/AHCI Mode/RAID **(bold** = default setting) - Short operational descriptions for each sub-menu setting can be found in the upper left corner of the BIOS set-up screen.
Serial-ATA Controller 0	Disabled/Enhanced/**Compatible**
Serial-ATA Controller 1	Disabled/**Enhanced**

If the SATA Mode selection is changed to the **AHCI Mode or RAID** then the following sub-menu options are available:

Option	Description
Supports Staggered Spin Up	**Disabled**/Enabled **(bold** = default setting) - Short operational descriptions for each sub-menu setting can be found in the upper left corner of the BIOS set-up screen.
Port 0 through 5 Hot Plug	**Disabled**/Enabled
External SATA Port 0 through 5	**Disabled**/Enabled

USB Configuration
The top portion of the menu screen lists the USB devices detected by the BIOS. The lower portion has several sub-menu selections available where you can set the parameters for the USB devices.

Option	Description
USB Support	**Enabled**/Disabled **(bold** = default setting) - Short operational descriptions for each sub-menu setting can be found in the upper left corner of the BIOS set-up screen.
Legacy USB Support	**Enabled**/Disabled
EHCI Hand-Off	**Disabled**/Enabled
Port 60/64 Emulation	**Enabled**/Disabled
USB Hardware Delays and Timeouts	The following sub-menu selections are used to configure data transfer delays and timeouts needed for the USB storage devices used in the system design: USB Transfer Timeout: 1 sec, 5 sec, 10 sec, **20sec** Device Reset Timeout: 10sec, **20sec**, 30sec, 40sec Device Power-Up Delay: ***Auto****, 1-40* Device Power-Up Delay in seconds: ***5****, Range of 1-40*

Info Report Configuration
Use this sub-menu to configure the available SHB BIOS post and error message reports.

Option	Description
Post Report	**Disabled**/Enabled **(bold** = default setting) - Short operational descriptions for each sub-menu setting can be found in the upper left corner of the BIOS set-up screen. If Enabled ► Delay Time: **5**/0-10 seconds/Until Press ESC
Error Message Report	**Disabled**/Enabled
Summary Screen	**Disabled**/Enabled If Enabled ► Delay Time: **5**/0-10 seconds/Until Press ESC

Super IO Configuration
The only Super IO component available in a system implementation using a JXT6966 or JXTS6966 is located on the optional IOB33 module. An IOB33 can plug into the SHBs' P20 I/O Expansion connector. If an IOB33 is plugged into the SHB then the Super IO Configuration submenu will be displayed. This Advanced Setup sub-menu allows you to configure the system ports connected to the IOB33s' Super I/O component.

NOTE: The following Super IO settings are only valid when an optional Trenton IOB33 I/O Board is installed on the JXT6966 or JXTS6966 SHB.

Floppy Disk Controller
This option allows you to enable or disable the floppy drive controller on your platform.

Option	Description
Disabled	Set this value to prevent the BIOS from detecting the onboard floppy drive controller.
Enabled (**bold** = default setting)	Set this value to allow the BIOS to use the onboard floppy drive controller. This is the default setting.
Change Settings	**Auto**/IO=3F0h/IRQ=6/DMA=1,2,3

Floppy Device Mode
This option allows you to enable or disable write-protection of floppy disks.

Option	Description
Read Write	Set this value to allow writing to floppy disks. This is the default setting.
Write Protect	Set this value to prevent writing to floppy disks.

Serial Port Configuration
This option specifies the base I/O port address and Interrupt Request address of serial port 0.

Option	Description
Serial Port 0	**Enabled**/Disabled **(bold** = default setting)
Change Settings	Auto / IO=3F8h; IRQ=4 / IO=3F8h; IRQ=3,4,5,6,7,10,11,12 / IO=2F8h; IRQ=3,4,5,6,7,10,11,12 / IO=3E8h; IRQ=3,4,5,6,7,10,11,12 / IO=2E8h; IRQ=3,4,5,6,7,10,11,12/
Device Mode	**Normal** / High Speed
3E8/IRQ4	Set this value to allow the serial port to use 3E8 as its I/O port address and IRQ 4 for the interrupt address. If the system will not use a serial device, it is best to set this port to *Disabled*.
2E8/IRQ3	Set this value to allow the serial port to use 2E8 as its I/O port address and IRQ 3 for the interrupt address. If the system will not use a serial device, it is best to set this port to *Disabled*.
Serial Port 1	**Enabled**/Disabled **(bold** = default setting)
Change Settings	Auto / IO=3F8h; IRQ=4 / IO=3F8h; IRQ=3,4,5,6,7,10,11,12 / IO=2F8h; IRQ=3,4,5,6,7,10,11,12 / IO=3E8h; IRQ=3,4,5,6,7,10,11,12 / IO=2E8h; IRQ=3,4,5,6,7,10,11,12/
Device Mode	Normal

Parallel Port Configuration

This option enables/disables the parallel port on the IOB33 and is used to configure the I/O address and operating mode for the parallel port. The default setting is AUTO, but you may elect to change this as needed.

Option	Description
Parallel Port	**Enable**/Disable - Set this value to *disable* prevent the parallel port from accessing any system resources. When the value of this option is set to *Disabled*, the printer port becomes unavailable. *Enabled* is the BIOS default setting
Change Settings	The default setting for this operation is ***AUTO***, which allows the board's BIOS to automatically assign system resources to the IOB33 parallel port. You may also select specific IO address and IRQ setting values from the list below: IO=378h; IRQ=5; IO=378h; IRQ=3,4,5,6,710,11,12; IO=278h; IRQ=3,4,5,6,710,11,12; IO=3BCh; IRQ=3,4,5,6,710,11,12; IO=378h; IO=278h; IO+3BCh; Note: The majority of parallel ports on computer systems use IRQ7 and I/O Port 378H as the standard setting.
Change Settings	The default setting for this operation is ***AUTO***, which allows the board's BIOS to automatically assign system resources to the IOB33 parallel port. You may also select specific IO address and IRQ setting values from the list below: IO=378h; IRQ=5; DMA=3 IO=378h; IRQ=3,4,5,6,710,11,12; DMA=1,3; IO=278h; IRQ=3,4,5,6,710,11,12; DMA=1,3; IO=3BCh; IRQ=3,4,5,6,710,11,12; DMA=1,3; IO=378h; DMA=1,3; IO=278h; DMA=1,3; IO+3BCh; DMA=1,3; Note: The majority of parallel ports on computer systems use IRQ7 and I/O Port 378H as the standard setting.
Device Mode	*Standard (STD) Printer Mode* is the default value for this print mode selection. Other parallel printer operating modes available are: SPP Mode EPP-1.9 and SPP Mode EPP-1.7 and SPP Mode ECP Mode ECP-1.9 and SPP Mode ECP-1.7 and SPP Mode The EPP modes enable the parallel port to be used with devices that adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bi-directional data transfer driven by the host device. The ECP modes enable the parallel port to be used with devices that adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve data transfer rates up to 2.5 Megabits per second. ECP provides symmetric bi-directional communication.

Serial Port Console Redirection Configuration

The SHB must have an optional IOB33 installed in order for the BIOS setting to apply. Serial port console redirection is available for use on the IOB33's COM0 and COM1 serial communication ports. When selected, the serial port console redirection configuration BIOS screen displays the following parameters.

Option	Description
COM0 Console Redirection	Enabled/ **Disabled** -- Default setting is ***Disabled***. Note: The console redirection settings shown below are only available if the *Enabled* option is selected.
COM0 Console Redirection Settings	Use this setting to specify how the host computer and the remote computer will exchange data via the COM0 port. Both computers need to have compatible settings. Here are the available COM0 settings: Terminal Type: VT100. VT100+, VT-UTF8, **ANSI** Bits per second: 9600, 19200, 38400, 57600, **115200** Data Bits: 7, **8** Parity: **None**, Even, Odd, Mark, Space Stop Bits: ***1***, *2* Flow Control: **None**, Hardware RTS/CTS, Software Xon/Xoff Resolution 100x31: ***Disabled***, *Enabled* Legacy OS Redirection: ***80x24***, *80x25*
COM1 Console Redirection	Enabled/ **Disabled** -- Default setting is ***Disabled***. Note: The console redirection settings shown below are only available if the *Enabled* option is selected.
COM1 Console Redirection Settings	Use this setting to specify how the host computer and the remote computer will exchange data via the COM1 port. Both computers need to have compatible settings. Here are the available COM1 settings: Terminal Type: VT100. VT100+, VT-UTF8, **ANSI** Bits per second: 9600, 19200, 57600, **115200** Data Bits: 7, **8** Parity: **None**, Even, Odd, Mark, Space Stop Bits: ***1***, *2* Flow Control: **None**, Hardware RTS/CTS, Software Xon/Xoff Resolution 100x31: ***Disabled***, *Enabled* Legacy OS Redirection: ***80x24***, *80x25*

This page intentionally left blank

Chapter 3 Chipset Configuration Setup

Introduction

The term "chipset" is a bit of a misnomer for the Trenton JXT6966 and JXTS6966. The "chipset" on these SHBs is really a single component called a "Platform Controller Hub" or PCH. Specifically, the Trenton JXT6966 and JXTS6966 both feature the Intel® 3420. This new PCH device combines many of the capabilities that were previously contained in individual North Bridge and South Bridge chipset components. The following section covers the set-up parameters of what could thought of as the North Bridge and South Bridge sections of the Intel® 3420 Platform Controller Hub.

North Bridge Configuration

The *North Bridge Configuration* menu item allows the user to do the following:

Option	Description
►Jasper Forest I/O Configuration	This option allows the user to view, enable or disable the Intel® Virtualization Technology for Directed I/O feature of the processors. The default setting is Disabled and when Enabled the following sub-menu of specific I/O parameters become available for selection; ►Intel® VT for Directed I/O Configuration ►Intel VT-d ***Disabled****/Enabled* (if Enabled the following five selections appear) Interrupt Remapping: ***Enabled****/Disabled* Coherency Support: **Disabled**/Enabled ATS Support: ***Enabled****/Disabled* Pass Through DMA: **Enabled**/Disabled ISOC: ***Disabled****/Enabled* **(bold** = default setting) Intel I/O AT: **Enabled**/Disabled DCA Support: ***Enabled****/Disabled* (cannot change) PCIe-Force Gen1: ***Disabled****/Enabled* IIO 0 NTB Configuration: **Transparent Bridge**/NTB to NTB/NTB to RP Primary Bar 23 Size: ***12****/1-38* Primary Bar 45 Size: ***12****/1-38* Secondary Bar 23 Size: ***12****/1-38* Secondary Bar 45 Size: ***12****/1-38* Secondary Bar 0/1 Prefetchable: ***Disabled****/Enabled* CrossLink Control Override: **Use NTMCROSSLINK pin**/DSD/USP/USD/DSP ASPM L0/L1 Configuration: **Disable L0 & L1**/Enable L0 only/ Enabled L0 and L1 L0 Maximum Acceptable Latency: **No Limit**/1us,2us/4us/8us/16us/32us/64us L0 Exit Latency: **>4is**/<64ns/>=64ns but <128ns/>=128ns but <256ns/ >=256ns but <512ns/>=512ns but <1is/>=1is but <2is/>=2is but <4is L1 Maximum Acceptable Latency: **No Limit**/1us/2us,4us/8us/16us/32us/64us/128us/ 256us/512us L1 Exit Latency: **>64us**/<1 us/>=1us but <2us/>=2us but <4us/>=4us but<8us >=8us but <16us/>=16us but <32us/>=32us but <64us IIO 1 NTB Configuration: **Transparent Bridge**/NTB to NTB/NTB to RP Primary Bar 23 Size: ***12****/1-38* Primary Bar 45 Size: ***12****/1-38* Secondary Bar 23 Size: ***12****/1-38* Secondary Bar 45 Size: ***12****/1-38* Secondary Bar 0/1 Prefetchable: ***Disabled****/Enabled* CrossLink Control Override: **Use NTMCROSSLINK pin**/DSD/USP/USD/DSP ASPM L0/L1 Configuration: **Disable L0 & L1**/Enable L0 only/ Enabled L0 and L1 L0 Maximum Acceptable Latency: **No Limit**/1us,2us/4us/8us/16us/32us/64us L0 Exit Latency: **>4is**/<64ns/>=64ns but <128ns/>=128ns but <256ns/ >=256ns but <512ns/>=512ns but <1is/>=1is but <2is/>=2is but <4is L1 Maximum Acceptable Latency: **No Limit**/1us/2us,4us/8us/16us/32us/64us/128us/ 256us/512us L1 Exit Latency: **>64us**/<1 us/>=1us but <2us/>=2us but <4us/>=4us but<8us >=8us but <16us/>=16us but <32us/>=32us but <64us

►QPI Link	This option allows the user to view, select or set to auto the frequency of the Intel® Quick Path Interconnect or Intel QPI link between processors. The default setting is Auto which allows the system to pick the optimum QPI frequency based on the processor type installed on the SHB. Other link settings are available for the user, but Trenton recommends using the QPI Link defaults. Current QPI Link Speed Mode: Fast (informational, depends on installed processors) Current QPI Frequency: 4.8GTs (informational, depends on installed processors) QPI Frequency Select: **Auto**/4.4GT/s/4.270 GT/s/Disable Fast Mode RTID Profile (UP): **Default**/UP IO-centric RTID Profile (DP/NUMA): **Default**/DP CPU-centric(NUMA)/DP IO-centric NUMA
Memory Information	The first five parameters listed below are informational in nature (i.e. they cannot be changed) and they reflect the memory DIMMs that were sensed by the BIOS upon power up: Total Memory: 6144MB (DDR) Current Memory Mode: Independent Current Memory Speed: 1067MHz Mirroring: Supported *or* Not Possible Sparing: Supported *or* Not Possible The following North Bridge function parameters may be changed: Memory Mode: **Independent**/Mirroring/Lock Step/Sparing (**bold** = default) NUMA: **Enabled**/Disabled Channel Interleaving: **6 Way**/Auto/4 Way/3 Way/2 Way/1 Way Rank Interleaving: **4 Way**/3 Way/2 Way/1 Way Hardware Memory Test: ***Disabled****/Enabled* Software Memory Test: *Disabled/****Enabled*** Patrol Scrub: **Disabled**/Enabled Demand Scrub: **Disabled**/Enabled Fast MRC: Disabled/**Enabled** DDR3 Memory Operating Speed: ***Auto****/1333MHz/1067MHz/800MHz* Memory Rank Margining: ***Disabled****/Enabled* Margin Ranks Loop Count (can't change): **15**/1-31 Closed Loop Throttling: ***Disabled****/Enabled* Temp Hysteresis: **1.5˚ C**/Disabled/3˚C/6˚ C Guard Band Temp: ***2****/1-99* Inlet Temp: ***70****/1-99* Temp Rise: ***0****/1-99* Air Flow: **1000**/500-5000 Altitude: ***0****/500-5000* DIMM Pitch: ***425****/350-500* Open Loop Throttling: ***Disabled****/Enabled* Inlet Temp: ***70****/1-99* Temp Rise: ***0****/1-99* Air Flow: **1000**/500-5000 Altitude: ***0****/500-5000* DIMM Pitch: ***425****/350-500*

►DIMM Information	The parameters listed below are informational in nature (i.e. they cannot be changed) and displays the total memory installed on the SHB as well as the memory size installed in each DDR3 Mini-DIMM socket on the board. The parameter results display below are examples of what could be displayed on this sub-menu. Node 0 DIMM Information Memory Channel 0 Memory CH 0 Slot 0: *2048 MB (DDR)* Memory CH 0 Slot 1: *Not Present* Memory Channel 1 Memory CH 1 Slot 0: *Not Present* Memory CH 1 Slot 1: *Not Present* Memory Channel 2 Memory CH 2 Slot 0: *Not Present* Memory CH 2 Slot 1: *Not Present* Node 1 DIMM Information Memory Channel 0 Memory CH 0 Slot 0: *2048 MB (DDR)* Memory CH 0 Slot 1: *Not Present* Memory Channel 1 Memory CH 1 Slot 0: *Not Present* Memory CH 1 Slot 1: *Not Present* Memory Channel 2 Memory CH 2 Slot 0: *Not Present* Memory CH 2 Slot 1: *Not Present*

South Bridge Configuration

The *South Bridge Configuration* menu item allows the user to do the following:

Option	Description
SMBus Controller	***Enabled****/Disabled* - This option allows the user to enable or disable the SMBus Controller in the Intel® 3420 ***(bold** = default)*
GbE Controller	***Enabled****/Disabled* - This option allows the user to enable or disable the Ethernet Controller in the Intel® 3420. Disabling this internal controller shuts down the LAN interface to the PICMG 1.3 backplane. This setting does not affect the operation of the independent Intel 82575 Ethernet Controller that drives the two LAN ports on the SHBs I/O plate.
Wake on LAN from S5	***Enabled****/Disabled* - This option allows the user to enable or disable wake on LAN feature derived from an ACPI S5 shutdown event
Restore AC Power Loss Settings	***Power On****/Power Off/Last State* - This option allows the user to determine how the system will come back up when power is restored after an unplanned power interruption. The options are Power Off, Power On or Last State.
SLP_S4 Assertion Stretch Enable	**Enabled**/Disabled
SLP_S4 Assertion Width	**4-5seconds**/1-2 Seconds/2-3 Seconds/3-4 Seconds
Azalia HD Audio	**Enabled**/Disabled
Azalia internal HDMI codec	**Enabled**/Disabled
High Precision Timer	**Enabled**/Disabled

PCI Express Ports Configuration	This option allows the user to Enable, Disable or Automatically turn on the various PCI Express ports inside the Intel® 3420 PCH. The default setting is set to Auto and Trenton highly recommends leaving this setting alone. These internal PCIe ports drive on-board components and turning them off will disable critical SHB and system functions PCI Express Port 1: **Auto**/Disabled/Enabled PCI Express Port 2: **Auto**/Disabled/Enabled PCI Express Port 3: **Auto**/Disabled/Enabled PCI Express Port 4: **Auto**/Disabled/Enabled PCI Express Port 5: **Auto**/Disabled/Enabled PCI Express Port 6: **Auto**/Disabled/Enabled PCI Express Port 7: **Auto**/Disabled/Enabled
USB Configuration	This option allows the user to Enable or Disable the various USB ports inside the Intel® 3420 PCH. The default setting is set to Enable. These internal USB ports drive the USB interface connections to the SHBs I/O plate and down to edge connector C for us on a PICMG 1.3 backplane. All USB Devices: **Enabled**/Disabled EHCI Controller 1: ***Enabled****/Disabled* EHCI Controller 2: ***Enabled****/Disabled* RMH Support: **Enabled**/Disabled/Auto (if disabled the following UHCI parameters become available) UHCI Controller 1: ***Enabled****/Disabled* UHCI Controller 2: ***Enabled****/Disabled* UHCI Controller 3: ***Enabled****/Disabled* UHCI Controller 4: *Enabled/****Disabled*** UHCI Controller 5: ***Enabled****/Disabled* UHCI Controller 6: *Enabled/****Disabled*** UHCI Controller 7: *Enabled/****Disabled*** USB Port 0: **Enabled**/Disabled USB Port 1: **Enabled**/Disabled USB Port 2: **Enabled**/Disabled USB Port 3: **Enabled**/Disabled USB Port 4: **Enabled**/Disabled USB Port 5: **Enabled**/Disabled USB Port 6: Enabled/**Disabled** USB Port 7: Enabled/**Disabled** USB Port 8: **Enabled**/Disabled USB Port 9: **Enabled**/Disabled USB Port 10: Enabled/**Disabled** USB Port 11: Enabled/**Disabled** USB Port 12: Enabled/**Disabled** USB Port 13: Enabled/**Disabled**

This page intentionally left blank

Chapter 4 Boot Setup

Introduction
Select the *Boot Setup* menu item from the Aptio TSE screen to enter the BIOS Setup screen. The Boot menu option allows you to access the following the following boot setup features.

Quite Boot
Set this value to allow the boot up screen options to be modified between POST messages or OEM logo.

Option	Description
Disabled (default)	Set this default value allows the computer system to display the POST messages.
Enabled	Set this value to allow the computer system to display the OEM logo.

Fast Boot

Option	Description
Disabled	Set this to allow the computer system to a full boot with a full set of devices. In full configuration mode, all devices are detected and initialized. This is the default setting.
Enabled	Set this value to allow the computer system to do a minimal boot. In minimal configuration mode, only the devices that are necessary to boot the system are detected and initialized.

Setup Prompt Timeout

Option	Description
Setup Prompt Timeout	**1 (default)** /Acceptable value range: 1-65535

Bootup NumLock State

Option	Description
On	Set this value to allow the Number Lock on the keyboard to be enabled automatically when the computer system is boot up. This allows the immediate use of 10-keys numeric keypad located on the right side of the keyboard. This is the default setting.
Off	This option does not enable the keyboard Number Lock automatically. To use the 10-keys on the keyboard, press the Number Lock key located on the upper left-hand corner of the 10-key pad.

The next four BIOS settings on this screen are:

- Gate20 Active: ***Upon Request****/Always*
- Option ROM Messages: ***Force BIOS****/Keep Current*
- Interrupt 19 Capture: ***Disabled****/Enabled*
- Non-EDID Monitor Support: *Disabled/****Enabled***

These are special purpose BIOS settings and should remain in the default positions. Contact Trenton's technical support team if you need to use these BIOS settings.

82575EB LAN1

Option	Description
Enabled	Set this value to enable Ethernet LAN1 on the SHB. This is the default setting.
Disabled	Set this value to disable Ethernet LAN1 on the SHB.

82575EB LAN2

Option	Description
Enabled	Set this value to enable Ethernet LAN2 on the SHB. This is the default setting.
Disabled	Set this value to disable Ethernet LAN2 on the SHB.

Onboard VGA

Option	Description
Onboard Video	Enabled (default) / Disabled

Primary Video Device

Option	Description
Primary Video	Off Board VGA (default) / Onboard VGA

Delay Before Bus Enumeration

Option	Description
Bus Enumeration	**None (default)** / Acceptable value range = 1 sec / 2secs / 3secs / 4secs / 5secs / 6secs / 7secs / 8secs / 9secs / 10secs

Boot Option Priorities

The following settings allow you to set the system boot priority of where to pull the BIOS settings from in order to perform a system boot. You can set three priority levels and the number of available options within each priority is based on the devices connected to the SHB. Here is an example of potential boot options.

Boot Option #1	Boot Option #2	Boot Option #3
SATA Hard Drive [HD type info]	Built-In EFI Shell	USB Flash Hub [USB type info]
Built-In EFI Shell	SATA Hard Drive [HD type info]	SATA Hard Drive [HD type info]
USB Flash Hub [USB type info]	USB Flash Hub [USB type info]	Built-In EFI Shell
Disabled	Disabled	Disabled

Any other devices connected to SHB and the system would show up under each option in the above listing similar to the SATA and USB devices in the example above.

Hard Drive BBS Priorities

BBS means BIOS Boot Specification and this BIOS setting is nearly identical to the Boot Option Priorities. The only difference is that the built-in EFI shell is not a boot option. The options are the devices connected to the system and the disabled option as listed in the example below.

Boot Option #1	Boot Option #2
SATA Hard Drive [HD type info]	USB Flash Hub [USB type info]
USB Flash Hub [USB type info]	SATA Hard Drive [HD type info]
Disabled	Disabled

This page intentionally left blank

Chapter 5 Security

Two Levels of Password Protection
Security Setup provides both an Administrator and a User password. If you use both passwords, the Administrator password must be set first.

The system can be configured so that all users must enter a password every time the system boots or when the BIOS Setup is executed using either the Administrator password or the User password.

If only the Administrator password is set, then this limits access to setup and is only asked for when entering setup. If only the User password is set, then this is a power-on password and must be entered to boot the SBC or to enter the board's BIOS setup screens. In setup the User will have administrator rights.

The Administrator and User passwords activate two different levels of password security. If you select password support, you are prompted for a one to six character password. Type the password on the keyboard. The password does not appear on the screen when typed. Make sure you write it down. If you forget it, you must drain NVRAM and reconfigure.

Remember the Password
Keep a record of the new password when the password is changed. If you forget the password, you must erase the system configuration information in NVRAM. See (Deleting a Password) for information about erasing system configuration information.

Security Setup
The *Security* setup menu item allows the user to do the following:

Option	Description
User Password	This option allows the user to set a user level password for the BIOS.
Administrator Password	This option allows the user to set an administrative level password for the BIOS.

This page intentionally left blank

Chapter 6 Saving and Exiting BIOS Setup and Restoring Defaults

Introduction
There are four methods of saving BIOS changes and leaving Aptio TSE listed at the top of this screen:

1 - **Save Changes & Exit**
When you have completed the system configuration changes, select this option to save your BIOS changes and leave Aptio TSE. You will need to reboot the computer for the new system configuration parameters to take effect.

Select Save Changes & Exit from the Exit menu and press <Enter>.

Save Configuration Changes and Exit Now?

[YES] [NO] appears in the window. Select *YES* to save changes and exit.

2 - **Discard Changes & Exit**
Select this option to quit Aptio TSE without making any permanent changes to the system configuration.

Select Discard Changes & Exit from the Exit menu and press <Enter>.

Discard Changes and Exit Setup Now?

[YES] [NO] Select *YES* to discard changes and exit.

3 - **Save Changes & Reset**
When you have completed the system configuration changes, select this option to save the BIOS changes, leave Aptio TSE and reset the computer so the new system configuration parameters can take effect.

Select Save Changes & Reset from the Exit menu and press <Enter>.

Save Configuration Changes and Exit Now?

[YES] [NO] appears in the window. Select *YES* to save changes and reset.

4 - **Discard Changes & Reset**
Choose this option if you decide to discard your BIOS changes, but what to reset the system upon leaving Aptio TSE.

Select Discard Changes & Reset from the Exit menu and press <Enter>.

Discard Configuration Changes and Exit Now?

[YES] [NO] appears in the window. Select *YES* to discard changes and reset.

The following two save options allow save or discard BIOS changes without leaving Aptio TSE:

Save Changes	[YES]	[NO]
Discard Changes	[YES]	[NO]

The following menu options for BIOS defaults are available:

Restore Defaults
Aptio TSE automatically sets all Aptio TSE options to a complete set of factory default settings when you select this option.

Select restore defaults from the Exit menu and press <Enter>.

Restore Defaults?

[YES] [NO] appears in the window. Select *YES* to load restore defaults.

Save as User Defaults
With this option the BIOS changes done so far by the user are saved as User Defaults.

Select save as user defaults from the Exit menu and press <Enter>.

Save as User Defaults?

[YES] [NO] appears in the window. Select *YES* to save user defaults.

Restore User Defaults
Aptio TSE automatically sets all Aptio TSE options to a complete set of user default settings when you select this option.

Select restore user defaults from the Exit menu and press <Enter>.

Restore User Defaults?

[YES] [NO] appears in the window. Select *YES* to load restore user defaults.

Boot Overide
Select this option to allow a system boot override from either a specific device; such as a hard drive, connected to the board or from the BIOS' EFI Shell.

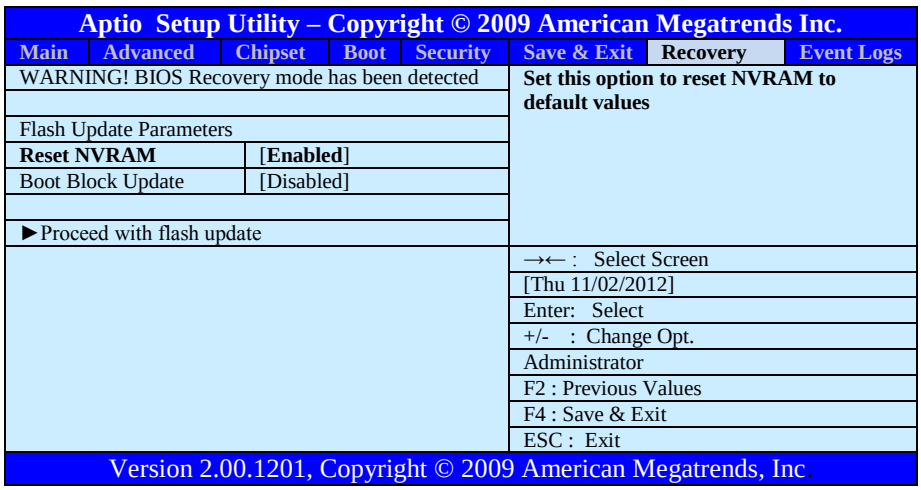
This page intentionally left blank

Chapter 7 BIOS Recovery

In order to recover the board's BIOS, several hardware conditions must be in place:

1. An optional IOB33 must be installed on the board
2. A PS/2 keyboard must be connected to the IOB33's keyboard/mouse port
3. The CRTL HOME keys must be tapped several times during boot to evoke the BIOS Recover menu

If these conditions are all satisfied then the RECOVERY option will be displayed in the BIOS setup menu as illustrated below.



Reset NVRAM
The choices for this setting are **Enabled**/Disabled with Enabled being the default setting. When enabled this option resets the NVRAM to the default values.

Boot Block Update
The choices for this setting are Enabled/**Disabled** with Disabled being the default setting. When enabled this option updates the boot block area of the firmware.

Proceed With Flash Update
Use caution when selecting this option because once selected the process of updating the system firmware is initiated. A secondary screen comes up to display a warning message and a flash update progress message. Here are the screen messages display when this selection is made:

WARNING! System firmware is being updated
Keyboard is locked.
DO NOT TURN THE POWER OFF!
Once the firmware update is completed, press any key to reboot the system.

Flash update is progress (status countdown is displayed here)

This page intentionally left blank

Chapter 8 SMBIOS Event Log

Change SMBIOS Event Log Settings
Use the Aptio TSE menu screen options to set up the system event log reporting format and configuration options for the BIOS.

Option	Description
►Change SMBIOS Event Log Settings	
SMBIOS Event Log	***Enabled****/Disabled* - This option allows the user to enable or disable the recoding of SMBIOS boot errors ***(bold** = default*
Erasing Settings	
Erase Event Log	***No****/Yes, Next Reset/Yes, Every reset* – Use this setting to control if and when to erase error messages for the event log.
When Log is Full	**Do Nothing**/Erase Immediately
SMBIOS Event Log Standard Settings	
MECI	***1****/1-255* - Multiple Event Count Increment – The number of duplicate occurrences of an event before the counter is updated
METW	***60****/0-99* - Multiple Event Time Window – The number of minutes that must pass between duplicate events before the counter is updated
Custom Options	
Log OEM Codes	**Enabled**/Disabled
Convert OEM Codes	**Disabled**/Enabled

View SMBIOS Event Log
This read-only menu screen displays the events recorded in the BIOS event log. An event's error code and severity along with the date and time that the event occurred are displayed on this screen.

This page intentionally left blank

Appendix A BIOS Messages

Introduction
A status code is a data value used to indicate progress during the boot phase. These codes are outputed to I/O port 80h on the SHB. Aptio 4.x core outputs checkpoints throughout the boot process to indicate the task the system is currently executing. Status codes are very useful in aiding software developers or technicians in debugging problems that occur during the pre-boot process.

Aptio Boot Flow
While performing the functions of the traditional BIOS, Aptio 4.x core follows the firmware model described by the Intel Platform Innovation Framework for EFI ("the Framework"). The Framework refers the following "boot phases", which may apply to various status code descriptions:

- Security (SEC) – initial low-level initialization
- Pre-EFI Initialization (PEI) – memory initialization[1]
- Driver Execution Environment (DXE) – main hardware initialization[2]
- Boot Device Selection (BDS) – system setup, pre-OS user interface & selecting a bootable device (CD/DVD, HDD, USB, Network, Shell, …)

[1] Analogous to "bootblock" functionality of legacy BIOS
[2] Analogous to "POST" functionality in legacy BIOS

BIOS Beep Codes
The Pre-EFI Initialization (PEI) and Driver Execution Environment (DXE) phases of the Aptio BIOS use audible beeps to indicate error codes. The number of beeps indicates specific error conditions.

PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
7	Reset PPI is not available
4	Recovery failed
4	S3 Resume failed

DXE Beep Codes

# of Beeps	Description
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
1	Invalid password
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

BIOS Status Codes

As the POST (Power On Self Test) routines are performed during boot-up, test codes are displayed on Port 80 POST code LEDs 0, 1, 2, 3, 4, 5, 6 and 7. These LED are located on the top of the SHB, just above the board's battery socket. The POST Code LEDs and are numbered from right (position 1 = LED0) to left (position 8 – LED7).

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following chart is a key to interpreting the POST codes displayed on LEDs 0 through 7 on the JXT6966 and JXTS6966 SHBs. Refer to the board layout in the *Specifications* chapter for the exact location of the POST code LEDs.

The HEX to LED chart in the POST Code LEDs section will serve as a guide to interpreting specific BIOS status codes.

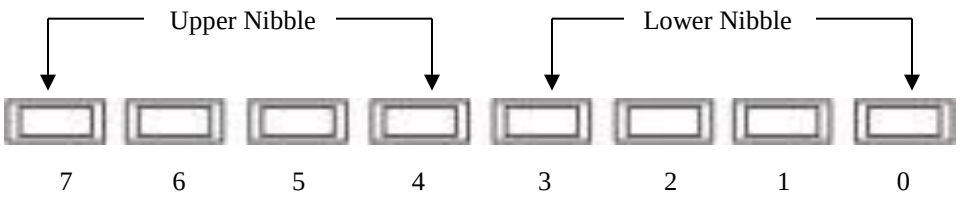
BIOS Status POST Code LEDs

As the POST (Power On Self Test) routines are performed during boot-up, test codes are displayed on Port 80 POST code LEDs 0, 1, 2, 3, 4, 5, 6 and 7. These LED are located on the top of the SHB, just above the board's battery socket. The POST Code LEDs and are numbered from right (position 1 = LED0) to left (position 8 – LED7).

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following chart is a key to interpreting the POST codes displayed on LEDs 0 through 7 on the JXT6966 and JXTS6966 SHBs. Refer to the board layout in the *Specifications* chapter for the exact location of the POST code LEDs.

Upper Nibble (UN)				
Hex. Value	LED7	LED6	LED5	LED4
0	Off	Off	Off	Off
1	Off	Off	Off	On
2	Off	Off	On	Off
3	Off	Off	On	On
4	Off	On	Off	Off
5	Off	On	Off	On
6	Off	On	On	Off
7	Off	On	On	On
8	On	Off	Off	Off
9	On	Off	Off	On
A	On	Off	On	Off
B	On	Off	On	On
C	On	On	Off	Off
D	On	On	Off	On
E	On	On	On	Off
F	On	On	On	On

Lower Nibble (LN)				
Hex. Value	LED3	LED2	LED1	LED0
0	Off	Off	Off	Off
1	Off	Off	Off	On
2	Off	Off	On	Off
3	Off	Off	On	On
4	Off	On	Off	Off
5	Off	On	Off	On
6	Off	On	On	Off
7	Off	On	On	On
8	On	Off	Off	Off
9	On	Off	Off	On
A	On	Off	On	Off
B	On	Off	On	On
C	On	On	Off	Off
D	On	On	Off	On
E	On	On	On	Off
F	On	On	On	On



JXT6966 & JXTS6966 POST Code LEDs

Status Code Ranges

Status Code Range	Description
0x01 – 0x0F	SEC Status Codes & Errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0xCF	DXE execution up to BDS
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

SEC Status Codes

Status Code	Description
0x0	Not used
Progress Codes	
0x1	Power on. Reset type detection (soft/hard).
0x2	AP initialization before microcode loading
0x3	North Bridge initialization before microcode loading
0x4	South Bridge initialization before microcode loading
0x5	OEM initialization before microcode loading
0x6	Microcode loading
0x7	AP initialization after microcode loading
0x8	North Bridge initialization after microcode loading
0x9	South Bridge initialization after microcode loading
0xA	OEM initialization after microcode loading
0xB	Cache initialization
SEC Error Codes	
0xC – 0xD	Reserved for future AMI SEC error codes
0xE	Microcode not found
0xF	Microcode not loaded

SEC Beep Codes

There are no SEC Beep codes associated with this phase of the Aptio BIOS boot process.

PEI Status Codes

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started

PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
S3 Resume Error Codes	
0xE8	S3 Resume Failed in PEI
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
7	Reset PPI is not available
4	Recovery failed
4	S3 Resume failed

DXE Status Codes

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)
0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization

0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)

0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

DXE Beep Codes

# of Beeps	Description
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
1	Invalid password
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

ACPI/ASL Status Codes

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

OEM-Reserved Status Code Ranges

Status Code	Description
0x5	OEM SEC initialization before microcode loading
0xA	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes